Abhijeet Upadhyay

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Education

- **Rajiv Gandhi Institute of Petroleum Technology** — Raebareli, India
  Bachelor of Technology - Electronics Engineering; CPI: 8.29 — *May 2024*
  Courses: *Analog Electronics, Digital Electronics, Data Structures and Algorithm, Microprocessor, Microelectronics*
- **Gyan Ganga Educational Academy** — Raipur (C.G), India
  Intermediate; Percentage: 90 — *May 2019*
- **Gyan Ganga Educational Academy** — Raipur (C.G), India
  Matriculation; CGPA: 10.0 — *May 2017*

Skills Summary

- **Languages**: C, C++, Python, Verilog HDL, VHDL
- **Tools**: magic VLSI, Xschem, Xilinx Vivado, ngspice, IRSIM, esim
- **Boards**: Arduino, Raspberry
- **Core**: Layout Design, Digital Design, PCB Design
- **Soft Skills**: Leadership, Writing, Public Speaking, Time Management

Internships

- **Summer Intern - IIT(BHU) Varanasi** — June 2022 - August 2022

  Worked on open-source EDA tools such ngspice, xschem, magic VLSI, and IRSIM for the layout design and simulation of simple CMOS-based circuits such as inverter, universal gates, multiplexers and latches. Used several PDKs(Process Design Kits) and technology files such as scmos and Skywater 130nm pdk. Used SKY130A technology file to design a RAM

Projects

- **Design of a simple Processor using VHDL**: Design of an 8-bit processor in VHDL based on a simple instruction set. Simulated on EDA playground. Creating testbench as well as design for specific simple instrucions such as addition, substraction and other logical and arithematic operations
- **Design and Implementation of Car parking System using Verilog**: This project aims at creating a parking system with multiple slots to mitigate the problem of tight parking spaces and high manual efforts to keep track of free space within a constrained area. The concept of the Finite State Machine is to be used to develop a smart car parking system. The design is implemented on Icarus Verilog which creates a RTL is further developed into a GDS file using digital design flow using open source tool qflow.
- **Layout Design of an 8-bit Potentiometric DAC**: The project is to design an 8-bit potentiometric DAC with 3.3v analog voltage, 1.8v digital voltage, and 1 off-chip external voltage reference using a sky130nm technology node on magic VLSi and xschem.
- **IoT-Based Alarm Clock System using NodeMCU ESP8266**: This project involves the creation of a touchless alarm clock that can be controlled through the Blynk App which is controlled by the ESP8266 module. The microcontroller ESP8266 is programmed using Ardunio IDE to take input from user from blynk app and output the alarm sound using a 5 Watt Speaker.
- **Covid-19 Hospital Management System**: C-based Covid hospital management system using file handling.In this project the data of the patient can be entered to know how many vaccine doses he/she has taken and print a certificate of vaccination for the patient.

Position of Responsibilities and achievements

- **Cleared JEE Advanced 2020**:
- **General Secretary at IEEE RGIPT Student Branch**:
- **Departmental Training and Placement Coordinator**: